WHAT IS CLAIMED IS:

1. A method of densifying a spacer oxide at least partially surrounding a polycide structure, said method comprising densifying said spacer oxide in a non-oxidizing ambient.

2. The method of claim 1, wherein said method comprises densifying said spacer oxide by exposing said spacer oxide to an oxide-densifying temperature for a period of time effective to densify said spacer oxide.

3. The method of claim 2, wherein said non-oxidizing ambient comprises a vacuum.

4. The method of claim 2, wherein said non-oxidizing ambient comprises a non-oxidizing gas.

5. The method of claim 4, wherein said non-oxidizing gas comprises at least one of nitrogen, argon, helium, deuterium, or a combination thereof.

6. The method of claim 5, wherein said non-oxidizing gas comprises nitrogen.

7. The method of claim 5, wherein a surface of said polycide structure is exposed to said non-oxidizing ambient during said densifying of said spacer oxide.

8. The method of claim 5, wherein at least a portion of said polycide structure is not encapsulated by silicon oxide or silicon nitride during said densifying of said spacer oxide.

9. The method of claim 8, wherein said polycide comprises tungsten silicide.

10. The method of claim 8, wherein said polycide suffers from substantially no adhesion loss following said densifying.

11. The method of claim 1, wherein said polycide structure comprises a part of a MOSFET semiconductor device.

12. The method of claim 11, wherein said polycide structure comprises a part of a CMOS semiconductor device.

13. The method of claim 11, wherein said polycide structure comprises a non-volatile memory polycide structure; wherein said device further comprises a non-memory polycide structure having a spacer oxide at least partially surrounding said non-memory polycide structure; and wherein said method further comprises densifying said spacer oxide at least partially surrounding said non-memory polycide structure in said non-oxidizing ambient simultaneously with densifying of said spacer oxide at least partially surrounding said non-volatile memory polycide structure.

14. A semiconductor device fabricated at least in part using the method of claim 1.

15. A method of forming a semiconductor structure on a substrate, comprising:

forming a polycide structure comprising at least one polysilicon layer and at least one metal silicide layer;

forming a spacer oxide on said polycide structure, said spacer oxide being formed to at least partially surround said polycide structure; and

densifying said spacer oxide in a non-oxidizing ambient to form said semiconductor structure.

16. The method of claim 14, wherein said polycide comprises tungsten silicide.

17. The method of claim 16, wherein said non-oxidizing ambient comprises nitrogen gas, and wherein said method comprises densifying said spacer oxide by exposing said spacer oxide to an oxide-densifying temperature for a period of time effective to densify said spacer oxide in said nitrogen gas.

18. The method of claim 17, wherein substantially no off-site oxide growth loss occurs due to oxidation of exposed silicon surfaces during said spacer densification.

19. The method of claim 17, wherein said oxide-densifying temperature comprises a temperature of from about 850 °C and about 1050 °C.

20. The method of claim 17, wherein said polycide structure comprises a part of a MOSFET semiconductor device.

21. The method of claim 20 wherein said semiconductor structure comprises a non-memory MOSFET control gate structure; and wherein said method further comprises forming a gate oxide on a semiconductor substrate and forming said polycide structure on said gate oxide, said gate oxide and said polycide structure together forming said non-memory control gate structure.

22. The method of claim 20, wherein said semiconductor structure comprises a MOSFET non-volatile memory structure; and wherein said method further comprises:

forming a memory oxide on a semiconductor substrate;

forming a doped floating gate polysilicon layer on said memory oxide;

forming an inter-poly oxide layer on said doped floating gate polysilicon layer; and

forming said polycide structure on said inter-poly oxide layer, said inter-poly oxide layer and said polycide structure together forming said non-memory control gate structure.

23. The method of claim 20, wherein said polycide structure comprises a part of a CMOS semiconductor device.

24. The method of claim 23, wherein said polycide structure comprises a non-volatile memory polycide structure; wherein said device further comprises a non-memory polycide structure having a spacer oxide at least partially surrounding said non-memory polycide structure; and wherein said method further comprises densifying said spacer oxide at least partially surrounding said non-memory polycide structure in said non-oxidizing ambient simultaneously with densifying said spacer oxide at least partially surrounding said non-volatile memory polycide structure.

25. A semiconductor device fabricated at least in part using the method of claim 15.

26. A method of forming a non-volatile memory stack structure and a non-memory control gate stack structure of an integrated semiconductor device on a silicon substrate, said method comprising:

forming a dielectric isolation region on said silicon substrate, said dielectric isolation region being formed between an active non-volatile memory mesa area and an active non-memory mesa area of said silicon substrate;

forming a memory cell oxide layer on said silicon substrate over said active non-volatile memory mesa area;

forming a doped floating gate polysilicon layer on said memory cell oxide layer over said active non-volatile memory mesa area;

forming an inter-poly oxide layer on said doped floating gate polysilicon layer over said active non-volatile memory mesa area;

forming a thin gate oxide layer on said silicon substrate over said active non-memory mesa area;

forming a doped control gate polysilicon layer on said thin gate oxide of said active non-memory mesa area and on said inter-poly oxide layer of said active non-volatile memory mesa area;

forming a refractory metal silicide layer on said doped control gate polysilicon layer over said active non-volatile memory mesa area so as to form a non-volatile memory stack structure over said active non-volatile memory mesa area;

forming heavily doped non-volatile memory source/drain regions of said non-volatile memory stack structure in said silicon substrate over said active non-volatile memory mesa area;

forming a refractory metal silicide layer on said doped control gate polysilicon layer over said active non-memory mesa area so as to form a non-memory control gate stack structure over said active non-memory mesa area;

forming lightly doped non-memory source/drain regions of said non-memory control gate stack structure in said silicon substrate over said active non-memory mesa area;

forming a spacer oxide side layer on each of said non-volatile memory stack and said non-memory control gate stack structures;

densifying said spacer oxide side layers in a non-oxidizing ambient; and

forming heavily doped non-memory source/drain regions of said non-memory control gate stack structure in said silicon substrate over said lightly doped non-memory source/drain regions.

27. The method of claim 26, wherein said method comprises:

forming said dielectric isolation region on said silicon substrate between said active non-volatile memory mesa area and said active non-memory mesa area of said silicon substrate;

then forming a memory cell oxide layer on said silicon substrate over said active non-volatile memory mesa area and said active non-memory mesa area of said silicon substrate;

then forming a doped floating gate polysilicon layer on said memory cell oxide layer;

then removing said doped floating gate polysilicon layer and said memory cell oxide layer from said active non-memory mesa area, leaving said doped floating gate polysilicon layer and said memory cell oxide layer on said active non-volatile memory mesa area;

then forming an inter-poly oxide layer on said doped floating gate polysilicon layer and over said dielectric isolation region and said active non-memory mesa area of said silicon substrate;

then removing said inter-poly oxide layer from said active non-memory mesa area, leaving said doped floating gate polysilicon layer and said inter-poly oxide layer over said active non-volatile memory mesa area;

then forming said thin gate oxide layer on said silicon substrate over said active non-memory mesa area;

then forming said doped control gate polysilicon layer on said thin gate oxide of said active non-memory mesa area and on said inter-poly oxide layer of said active non-volatile memory mesa area;

then forming said refractory metal silicide layer on said doped control gate polysilicon layer;

then forming an anti-reflective layer on said refractory metal silicide layer;

selectively removing areas of said doped floating gate polysilicon layer, said inter-poly oxide layer, said doped control gate polysilicon layer, said refractory metal silicide layer and said anti-reflective layer to form said non-volatile memory stack structure over said active non-volatile memory mesa area;

forming said heavily doped non-volatile memory source/drain regions of said non-volatile memory stack structure in said silicon substrate over said active non-volatile memory mesa area;

selectively removing areas of said doped control gate polysilicon layer, said refractory metal silicide layer and said anti-reflective layer to form said non-memory control gate stack structure over said active non-memory mesa area;

forming said lightly doped non-memory source/drain regions of said non-memory control gate stack structure in said silicon substrate over said active non-memory mesa area;

forming a thin oxide layer on the sidewalls of said non-volatile memory stack and on the sidewalls of said non-memory control gate stack;

forming said spacer oxide side layer on each of said non-volatile memory stack and said non-memory control gate stack structures, and removing at least a portion of each of said cell memory oxide and said thin gate oxide layers in a manner so that at least a portion of each of said heavily doped non-volatile memory source/drain regions, said lightly doped non-memory source/drain regions, said non-volatile memory stack anti-reflective layer and said non-memory control gate stack anti-reflective layer are substantially exposed;

densifying said spacer oxide side layers in a non-oxidizing ambient, wherein at least a portion of each of said heavily doped non-volatile memory source/drain regions, said lightly doped non-memory source/drain regions, said non-volatile memory stack anti-reflective layer and said non-memory control gate stack anti-reflective layer are substantially exposed during said densification; and

after said spacer densification forming said heavily doped non-memory source/drain regions of said non-memory control gate stack structure in said silicon substrate over said substantially exposed lightly doped non-memory source/drain regions.

28. The method of claim 26, wherein said refractory metal silicide comprises tungsten silicide, and wherein said non-oxidizing ambient comprises nitrogen gas.

29. The method of claim 28, wherein said integrated circuit device comprises a CMOS semiconductor device.

30. The method of claim 29, wherein said integrated circuit device comprises a one time programmable CMOS memory device.

31. The method of claim 30, wherein said tungsten silicide is formed by sputter deposition.

32. The method of claim 31, wherein said anti-reflective layer comprises a layer of silicon oxynitride formed by plasma enhanced chemical vapor deposition.

33. The method of claim 30, wherein said thin oxide layer is thermally grown on the sidewalls of said non-volatile memory stack and said non-memory control gate stack, and wherein substantially no thin oxide layer is thermally grown on the substantially exposed surface of said anti-reflective layer.

34. The method of claim 30, wherein said spacer oxide side layers are formed by depositing a layer of spacer oxide using TEOS chemical vapor deposition and then blanket etching said spacer oxide to form said oxide side layers and to substantially remove said oxide layer from surfaces of said non-volatile memory stack anti-reflective layer and said non-memory control gate stack anti-reflective layer; and wherein said etching further comprises overetching to remove at least a portion of said cell memory oxide and said thin gate oxide layers from at least a portion of each of said heavily doped non-volatile memory source/drain regions and said lightly doped non-memory source/drain regions.

35. The method of claim 30, wherein during said spacer densification substantially no oxide is grown in the substantially exposed surfaces of said heavily doped non-volatile memory source/drain regions and said lightly doped non-memory source/drain regions.

36. The method of claim 28, wherein said spacer densification is performed by rapid thermal processing at a temperature of from about 850 °C and about 1050 °C for a period of time effective to densify said spacer oxide side layers.

37. The method of claim 31, wherein said sputter deposition of said tungsten silicide is implemented in a conventional CMOS fabrication using a physical vapor deposition tungsten silicide chamber added to a conventional cluster-tool.

38. A semiconductor device fabricated at least in part using the method of claim 26.

39. A one time programmable CMOS memory device fabricated at least in part using the method of claim 30.